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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/022,226	12/17/2001	Harry Hedler	MAS-FIN-193	4181

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EXAMINER	
BEREZNY, NEMA O	

ART UNIT	PAPER NUMBER
2813	

DATE MAILED: 09/14/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/022,226	HEDLER ET AL.	
	Examiner	Art Unit	
	Nema O Berezny	2813	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *06 July 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-47* is/are pending in the application.

4a) Of the above claim(s) *15-40* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-14 and 41-47* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *17 December 2001* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *06142004*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Continued Examination Under 37 CFR 1.114

A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on 7-6-04 has been entered.

Claims 1-47 are currently pending.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1-2, 4-5, 7-9, 11-12, 14, and 41 are rejected under 35 U.S.C. 102(b) as being anticipated by Nolan et al. (5,508,228). Nolan discloses an electronic component, comprising: an electronic circuit (Figs.1,5a-5i el.12) having a first surface; electrical contacts (el.44) at least on said first surface for electrical bonding of said electronic circuit; at least one elevation (el.24) disposed on said first surface, said at least one elevation having an elevation surface and a contact zone, said at least one elevation

being formed of an insulating material having sufficient flexibility to absorb stresses occurring in said contact zone as a result of at least one of the group consisting of thermal loading and mechanical loading (col.7 lines 56-60), and said at least one elevation having a geometrical shape for achieving a spring-effect in directions extending parallel to said first surface (Fig.5d; col.8 lines 58-65 – as per Applicant's specification, p.18 lines 9-20 and Fig.2); at least one of said electrical contacts disposed on said at least one elevation (Fig.5i); and a conduction path (el.40) disposed on said elevation surface between said at least one of said electrical contacts and said electronic circuit **[claim 1]**. Nolan also discloses an insulating layer (el.34) at least partially covering said first surface and adjoining said at least one elevation (Fig.5i); and conductor runs (el.40) disposed on said insulating layer and forming a conducting connection between said at least one elevation and said electronic circuit (Fig.5i) **[claim 2]**; wherein said insulating layer is elastic (el.34) **[claim 4]**; wherein the electronic component is a semiconductor component (col.5 lines 27-33) **[claim 5]**; wherein at least one of said electrical contacts is formed by one of the group consisting of a conducting layer, a conducting pin, and a conducting ball (Fig.5i) **[claim 7]**; and wherein said elevation is taller than it is wide (Fig.5d; col.8 lines 58-65) **[claim 41]**.

Nolan also discloses an electronic component, comprising: an electronic circuit (el.12) having a first surface; electrical contacts (el.44) at least on said first surface for electrical bonding of said electronic circuit; at least one elevation (el.24) disposed on said first surface, said at least one elevation having a contact zone and an interior, said at least one elevation being formed of an insulating material having sufficient flexibility

to absorb stresses occurring in said contact zone as a result of at least one of the group consisting of thermal loading and mechanical loading (col.7 lines 56-60); at least one of said electrical contacts disposed on said at least one elevation (Fig.5i); and a conduction path (el.40) disposed in said interior between said at least one of said electrical contacts and said electronic circuit **[claim 8]**; an insulating layer (el.34) at least partially covering said first surface and adjoining said at least one elevation (Fig.5i); and conductor runs (el.40) disposed on said insulating layer and forming a conducting connection between said at least one elevation and said electronic circuit (Fig.5i) **[claim 9]**; wherein said insulating layer is elastic (el.34) **[claim 11]**; wherein the electronic component is a semiconductor component (col.5 lines 27-33) **[claim 12]**; and wherein at least one of said electrical contacts is formed by one of the group consisting of a conducting layer, a conducting pin, and a conducting ball (Fig.5i) **[claim 14]**.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 3 and 10 are rejected under 35 U.S.C. 103(a) as being unpatentable over Nolan as applied to claims 1-2 and 8-9 above, and further in view of Chen et al. (5,910,687). Nolan does not disclose an insulating layer at least partially covering said

at least one elevation. However, Nolan would look to one such as Chen for reliability of the contact layer because Chen discloses an insulating layer at least partially covering said at least one elevation (Fig.11 el.321). Therefore, it would have been obvious to a person of ordinary skill in the art at the time of the invention to use the insulating layer of Chen with the electronic component of Nolan in order to increase the reliability of the contact layer (Chen – col.10 lines 43-54).

Claims 6 and 13 are rejected under 35 U.S.C. 103(a) as being unpatentable over Nolan as applied to claims 1, 5, 8, and 12 above, and further in view of Lee et al. (6,140,456). Nolan does not disclose a polymer component. However, Nolan would look to one such as Lee for thin film material with a low dielectric constant because Lee discloses wherein the electronic component is a polymer component (col.1 lines 25-31; col.4 lines 29-42). Therefore, it would have been obvious to a person of ordinary skill in the art at the time of the invention to use the polymer component of Lee with the electronic component of Nolan in order to form a thin film of material with a low dielectric constant (col.4 lines 35-42; col.5 lines 24-42).

Claims 42-43 are rejected under 35 U.S.C. 103(a) as being unpatentable over Nolan (5,508,228) in view of Yoshifumi (JP 1-187948). Nolan discloses an electronic component, comprising: an electronic circuit (Figs.1,5a-5i el.12) having a first surface; electrical contacts (el.44) at least on said first surface for electrical bonding of said electronic circuit; at least one elevation (el.24) disposed on said first surface, said at

least one elevation having an elevation surface and a contact zone, said at least one elevation being formed of an insulating material having sufficient flexibility to absorb stresses occurring in said contact zone as a result of at least one of the group consisting of thermal loading and mechanical loading (col.7 lines 56-60); at least one of said electrical contacts disposed on said at least one elevation (Fig.5i); and a conduction path (el.40) at least partially covering said at least one elevation between said at least one of said electrical contacts and said electronic circuit (Fig.5i). However, Nolan does not disclose an insulation layer that only partially covers said at least one elevation. Nolan would look to one such as Yoshifumi for reducing deviation of the bump height because Yoshifumi discloses an insulation layer that only partially covers at least one elevation and leaves an outwardly facing surface free of said insulating layer (Figs.1-2 el.5b). Therefore it would have been obvious to a person of ordinary skill in the art at the time of the invention to use the insulation layer of Yoshifumi with the electronic component of Nolan in order to reduce deviation of the bump height (purpose), and to provide an electrical path to the electronic circuit.

Claim 44 is rejected under 35 U.S.C. 103(a) as being unpatentable over Nolan in view of Yoshifumi as applied to claim 42 above, and further in view of Bunting et al. (3,641,254). Nolan and Yoshifumi disclose at least one of said electrical contacts is disposed on said insulating layer; and a conduction path is disposed on said rough regions of said insulating surface between said at least one of said electrical contacts and said electrical circuit. However, Nolan and Yoshifumi do not disclose an insulating

layer with rough regions. Nolan and Yoshifumi would look to one such as Bunting for improved film contact because Bunting discloses an insulating layer with a rough region (col.3 lines 5-8). Therefore, it would have been obvious to a person of ordinary skill in the art at the time of the invention to use the rough regions of Bunting with the electronic component of Nolan and Yoshifumi in order to improve contact of the conductive film to the insulating layer (Bunting - col.3 lines 5-8).

Claim 45 is rejected under 35 U.S.C. 103(a) as being unpatentable over Nolan et al. (5,508,228) in view of Bunting et al. (3,641,254). Nolan discloses an electronic component, comprising: an electronic circuit (Figs.1,5a-5i el.12) having a first surface; electrical contacts (el.44) at least on said first surface for electrical bonding of said electronic circuit; at least one elevation (el.24) disposed on said first surface, said at least one elevation including an elevation surface and a contact zone, said at least one elevation being formed of an insulating material having sufficient flexibility to absorb stresses occurring in said contact zone as a result of at least one of the group consisting of thermal loading and mechanical loading (col.7 lines 56-60); at least one of said electrical contacts disposed on said elevation surface (Fig.5i); and a conduction path (el.40) disposed on said elevation surface between said at least one of said electrical contacts and said electronic circuit. However, Nolan does not disclose an insulating layer with rough regions. Nolan would look to one such as Bunting for improved film contact because Bunting discloses an insulating layer with a rough region (col.3 lines 5-8). Therefore, it would have been obvious to a person of ordinary skill in

the art at the time of the invention to use the rough regions of Bunting with the electronic component of Nolan in order to improve contact of the conductive film to the insulating layer (Bunting - col.3 lines 5-8).

Claims 46-47 are rejected under 35 U.S.C. 103(a) as being unpatentable over Nolan in view of Bunting as applied to claim 45 above, and further in view of Reetz et al. (6,309,798). Nolan and Bunting do not disclose rough regions including nuclei. However, Nolan and Bunting would look to one such as Reetz for a simple inexpensive process to improve film contact because Reetz discloses wherein said rough regions include nuclei (col.3 lines 37-57), and wherein the nuclei are palladium (col.4 lines 29-35). Therefore, it would have been obvious to a person skilled in the art at the time of the invention to use the nuclei made of palladium of Reetz with the electronic component of Nolan and Bunting. The roughened surface of Nolan and Bunting could be formed by a simple and inexpensive process (Reetz - col.5 line 56 – col.6 line 4).

Response to Arguments

Applicant's arguments with respect to claims 1-14 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Nema O Berezny whose telephone number is (571) 272-1686. The examiner can normally be reached on M-F 9-5:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Carl Whitehead, Jr. can be reached on (571) 272-1702. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

NB

Nema Berezny